IN THE CLAIMS

Please cancel claims 1-30.

Please add claims 31-60.

~~Patent claims~~ WHAT IS CLAIMED IS:

1-30. (Cancelled).

31. (New) An electronic component comprising:

a housing package comprising a plurality of layers of plastic;

at least one buried interconnect layer; and

at least one semiconductor chip, which has pointed-conical external contacts distributed on an outer side, the pointed-conical external contacts penetrating through one of the layers of plastic in the housing package and forming contact vias to the buried interconnect layer.

32. (New) The electronic component of claim 31, comprising:

wherein the electronic component is a multichip module with a number of buried interconnect layers and a number of semiconductor chips that have pointed-conical external contacts, the pointed-conical external contacts of the semiconductor chips in the housing package penetrating through different layers of plastic and forming contact vias with respect to different buried interconnect layers.

33. (New) The electronic component of claim 31, comprising the electronic component having buried semiconductor chips.

34. (New) The electronic component of claim 31, comprising the electronic component has thinned semiconductor chips with a thickness of between 30 and 100 micrometers as buried semiconductor chips.

35. (New) The electronic component of claim 32, comprising wherein the multichip module has external contact areas on the underside and/or the upper side.

36. (New) The electronic component of claim 32, comprising:

wherein the multichip module has semiconductor chips on its upper side, the chips penetrating with their pointed-conical external contacts through the uppermost layer of plastic and forming contact vias to a buried interconnect layer.

37. (New) The electronic component of claim 32, comprising wherein the multichip module has passive components on its upper side, the components being connected by means of contact vias in the uppermost layer of plastic to one of the buried interconnect layers.

38. (New) An electronic component comprising:

a housing package comprising a plurality of layers of plastic;

at least one buried interconnect layer; and

at least one semiconductor chip, which has pointed-conical external contacts distributed on an outer side, the pointed-conical external contacts penetrating through one of the layers of plastic in the housing package and forming contact vias to the buried interconnect layer,

wherein a hollow housing package has the layers of plastic, the buried interconnect layer and the at least one semiconductor chip, one of the layers of plastic forming a covering with contact vias and a further layer of plastic comprising the frame of the hollow housing package, which is penetrated by the pointed-conical external contacts of the semiconductor

chip, the pointed-conical external contacts being electrically connected to contact vias of the covering.

39. (New) The electronic component of claim 38, comprising wherein the hollow housing package is a light sensor housing or chip camera housing and the covering has a transparent layer of plastic.

40. (New) The electronic component of claim 39, comprising wherein the hollow housing package is a pressure sensor housing and the covering has a central opening for pressure coupling.

41. (New) The electronic component of claim 38, comprising wherein the hollow housing package is a gas sensor housing and the covering has a central opening for gas exchange.

42. (New) The electronic component of claim 38, comprising wherein the hollow housing package is a sound sensor housing and the covering has a central opening for receiving sound or emitting sound.

43. (New) The electronic component of claim 38, comprising wherein at least one of the layers of plastic has a pre-crosslinked plastic.

44. (New) The electronic component of claim 38, comprising wherein at least one of the layers of plastic has glass fiber or carbon fiber reinforcements.

45. (New) A panel with a number of component positions, the panel comprising:
a number of layers of plastic;
at least one buried interconnect layer; and

each component position having at least one semiconductor chip with pointed-conical external contacts distributed on an outer side, and the pointed-conical external contacts in the panel penetrating through one of the layers of plastic and forming contact vias to the buried interconnect layer.

46. (New) The panel of claim 45, comprising wherein each component position comprises a multichip module with a number of buried interconnect layers and a number of semiconductor chips, which have pointed-conical external contacts, the pointed-conical external contacts of the semiconductor chips penetrating through different layers of plastic in the panel and forming contact vias to different buried interconnect layers.

47. (New) The panel of claim 45, comprising wherein the panel has buried semiconductor chips.

48. (New) The panel of claim 45, comprising wherein the panel has thinned semiconductor chips with a thickness of between 30 and 100 micrometers as buried semiconductor chips.

49. (New) The panel of claim 45, comprising wherein the panel has external contact areas in each component position on the underside and/or the upper side.

50. (New) The panel of claim 45, comprising wherein the panel has semiconductor chips in each component position on its upper side, the chips penetrating with their pointed-conical external contacts through the uppermost layer of plastic and forming contact vias to a buried interconnect layer.

51. (New) The panel of claim 45, comprising wherein the panel has passive components on its upper side, the components being connected by means of contact vias in the uppermost layer of plastic to one of the buried interconnect layers.

52. (New) The panel of claim 45, comprising wherein the panel has in one of the layers of plastic a depression for a hollow housing package in each component position, with at least one buried interconnect layer and with at least one semiconductor chip, a further one of the layers of plastic forming a covering with contact vias.

53. (New) The panel of claim 45, comprising wherein the panel has at least one layer of plastic of a pre-crosslinked plastic.

54. (New) The panel of claim 45, comprising wherein the panel has at least one layer of plastic with glass fiber or carbon fiber reinforcements.

55. (New) A method for producing at least one electronic component comprising:

defining the electronic component to include a housing package comprising a number of layers of plastic, with at least one buried interconnect layer and with at least one semiconductor chip, which has pointed-conical external contacts disposed on an outer side, the pointed-conical external contacts penetrating through one of the layers of plastic in the housing package and forming contact vias to the buried interconnect layer;

producing a circuit carrier with external contact areas on the underside of the circuit carrier and an interconnect layer on the upper side of the circuit carrier, the external contact areas and the interconnect layer being electrically connected by means of contact vias through the circuit carrier;

producing semiconductor chips with pointed-conical external contacts;

applying a pre-crosslinked layer of plastic to the interconnect layer of the circuit carrier;

penetrating the pre-crosslinked layer of plastic with the pointed-conical external contacts of at least one of the semiconductor chips until the pointed-conical external contacts form contact vias to the interconnect layer and the at least one semiconductor chip is impressed in the pre-crosslinked layer of plastic;

curing and crosslinking the pre-crosslinked layer of plastic to form a layer of plastic; and

functional testing of the electronic component by means of the external contact areas of the circuit carrier.

56. (New) The method of claim 55, comprising, before the curing and crosslinking of the pre-crosslinked layer of plastic, applying a further pre-crosslinked layer of plastic to cover the semiconductor chip.

57. (New) The method of claim 55, comprising applying a structured pre-crosslinked layer of plastic with at least one depression for a hollow housing package to the interconnect layer of the circuit carrier.

58. (New) The method of claim 55, comprising applying a number of sequences of interconnect layers and layers of plastic with contact vias and embedded semiconductor chips to the interconnect layer of the circuit carrier, the pointed-conical external contacts of the semiconductor chip respectively penetrating through one of the layers of plastic and forming contact vias to one of the interconnect layers.

59. (New) The method of claim 55, comprising applying an upper interconnect layer, which is loaded with semiconductor chips and/or passive components to form a multichip module, to an uppermost layer of plastic.

60. (New) The method of claim 55, comprising dividing the panel up into individual electronic components.